

In the Claims

1. (Currently amended) A performance monitor for monitoring ~~the~~ an occurrence of incidences of one or more events related to ~~the~~ operation of a processor, comprising:

at least one monitor mode control register; and

a plurality of performance monitor counters operatively connected to said at least one monitor mode control register to count incidences of said one or more events, said at least one monitor mode control register grouping said performance monitor counters so that when one of said performance monitor counters reaches capacity in connection with the counting incidences of a first of said one or more events, a second of said performance monitor counters begins counting subsequent incidences of said first of said one or more events;

wherein the number of events equals X, and the number of performance monitor counters equals Y, whereby said at least one monitor mode control register groups said performance monitor counters into Z groups, wherein $Y/X=Z$; and

wherein when $X < Y$, said at least one monitor mode control register assigns a number of performance monitor counters, said number equal to an integer resulting from dividing Y by X, to each of said events to be counted; and

assigns any unassigned performance monitor counters to at least one of said events.

2. (Canceled)

3. (Currently amended) A performance monitor for monitoring ~~the~~ an occurrence of incidences of one or more events related to ~~the~~ operation of a processor, comprising:

at least one control element; and

a plurality of counting elements operatively coupled to said at least one control element to count incidences of said one or more events, said at least one control element grouping said plurality of counting elements so that when one of said plurality of counting elements reaches capacity in connection with the counting of incidences of a first of said one or more events, a second of said plurality of counting elements begins counting subsequent incidences of said first of said one or more events;

wherein the number of events equals X, and the number of counting elements equals Y, whereby said at least one control element groups said performance monitor counters into Z groups, wherein $Y/X=Z$; and

wherein when $X < Y$, said at least one control element assigns a number of counting elements, said number equal to an integer resulting from dividing Y by X, to each of said events to be counted; and

assigns any unassigned counting elements to at least one of said events.

4. (Original) The performance monitor as set forth in claim 3, wherein said at least one control element comprises a monitor mode control register.

5. (Currently amended) The performance monitor as set forth in claim 4, wherein each of said plurality of counting elements comprises a performance monitor counter operatively connected to said monitor mode control register.

6. (Canceled)